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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete if Known

Application Number 09/773,246

Filing Date February 1, 2001

First Named Inventor: David Robert Cameron Rolston
Serial Number: 6621

Group Art Unit 2031
Examiner Name

Examiner Name

Attorney Socket Name

Attorney Docket Number AP566US

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

Examiner
Signature

Date Considered

~~6/29/04~~

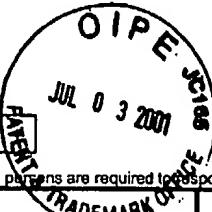
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	2	of	2	Attorney Docket Number	AP566US
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Complete if Known

Application Number	09/773,246
Filing Date	February 1, 2001
First Named Inventor	David Robert Cameron Rolston
Group Art Unit	2631
Examiner Name	

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	2A	"A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessors", by I.A. Young, J.K. Greason, & K.L. Wong, in IEEE Journal of Solid-State Circuits, Vol. 27, No. 11, November 1992, pp. 1599-1606.	
	2B	"Simultaneous Bidirectional Receiver Logic", by Kanichi Ishibashi et al. in IEEE Micro, Jan.-Feb. 1999, pp. 14-18.	
	2C	"Scaling Optoelectronic-VLSI Circuits into the 21st Century: A Technology Roadmap", by A.V. Krishnamoorthy & D.A. Miller, in IEEE J. of Selected Topics in Quantum Electronics, Vol. 2, No. 1, April 1996, pp. 55-76.	
	2D	"Optical Receivers for Optoelectronic VLSI", by T.K. Woodward, A.V. Krishnamoorthy, A.L. Lentine & L.M.F. Chirovski, in IEEE J. of Selected Topics in Quantum Electronics, Vol. 2, No. 1, April 1996, pp. 106-116.	
	2E	"Optical Control of Distributed Actuator and Sensor Arrays" by B. Bamieh, F. Paganini and M. Dahleh, in SPIE, Vol. 3323, March 1998, pp. 467-478.	
	2F	"Optical clock distribution to silicon chips" by B.D. Clymer and J.W. Goodman, in Optical Engineering, Vol. 25, No. 10, October 1986, pp. 1103-1108.	
	2G	"A Synchronous Approach for Clocking VLSI Systems" by F. Anceau, in IEEE Journal of Solid-State Circuits, Vol. SC-17, No. 1, February 1982, pp. 51-56.	
	2H	"Clock Distribution Using Coupled Oscillators", by I. Galton, D.A. Towne, J.J. Rosenberg and H.T. Jensen, in IEEE, 0-7803-3073-0-96, 1996, pp. 217-220.	
	2I	"The Composite Banyan Network" by S-W Seo and T-Y Feng, in IEEE Transactions on Parallel and Distributed Systems, Vol. 6, No. 10, October 1995, pp. 1043-1053.	

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